METHOD OF MARGINAL ERASURE FOR THE TESTING OF FLASH MEMORIES

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention generally relates to a method used in semiconductor memory manufacturing and, more particularly, to a method of erasing memory cells during testing in a flash electrically erasable programmable read only memory (EEPROM) in the fabrication of integrated circuits (ICs).

(2) Description of Prior Art

Electrically erasable EEPROMs, often referred to as "Flash" EPROM, have emerged as an important non-volatile memory. Having the same cell density as standard EPROMs, they have the advantage over EPROMs that they need not be exposed to ultraviolet (UV) light to be erased. This is also an advantage in that standard IC packages can be used for these devices whereas standard EPROMs require a special package allowing the IC die to be exposed to UV light.

In a standard Flash EPROM, a plurality of flash memory cells are arranged in an array of rows and columns. Refer now to Fig. 1 showing a typical flash memory cell device. Each cell 10 is composed of a p-type substrate 12 and separate n-type source 14

and drain 16 regions formed on the substrate 12. A p-type channel region 18 in the substrate 12 separates the source 14 and drain 16. A floating gate 20, electrically isolated from and positioned over the channel region 18, is separated from the substrate 12 by a thin dielectric layer 22. A control gate 24 is separated from the floating gate 20 by a second dielectric layer 26.

To program the flash EPROM cell, the drain and control gate are raised to voltages above the voltage applied to the source region. For example, the drain voltage (V_D) and control gate voltage (V_{CG}) are set to 5.5V and 9V above the source voltage, respectively. This produces hot electrons, which are transferred across the thin dielectric layer, trapping them on the floating gate. The control gate voltage threshold is the minimum voltage that must be applied to the control gate in order to affect conduction between the source and drain. This injection of hot electrons has the effect of raising the control gate threshold by about two to four volts.

To erase a flash EPROM cell, the source voltage (V_S) is set to a positive voltage and the control gate voltage (V_{CG}) is set to a negative voltage while the drain floats. Typically, the minimum normal source to control gate erase voltage (V_{NE}) is 11 volts. An electric field forms between the source and floating gate thereby removing the negative charge on the floating gate by Fowler-Nordheim tunneling. The minimum erase voltage increases with the number of program and erasure cycles performed. This is depicted in Fig. 2 where the minimum erase voltage is approximately 11.2V at the time of manufacturing and increases to just under 13V after 90,000 erasures. In order to

predict the proper operation of the device over the device lifetime, a lower voltage such as 12V is typically used during chip probe testing. This lower voltage test is referred to as marginal erase. If the memory will erase at this lower voltage at wafer probe, then it is statistically predicted that it will continue to erase at V_{NE} for many thousands of erasures.

Fig. 3 schematically shows how the normal and margin erase voltages are typically generated. During normal operation, an erase voltage V_E is generated from a charge pump circuitry and regulated by a regulator in the flash macro 42. For marginal erase testing, a fixed external voltage (V_{ME}) is applied to a test pad (30) to perform the marginal erase. V_{ME} is applied through resistor 32 by closing a switch 44 within the flash macro 42. Unfortunately, this requires placement of the additional test pad 30 to apply the marginal erase voltage (V_{ME}) during chip probe. In addition, since V_{ME} is fixed, it cannot compensate for changes observed in the normal erase voltage (V_{NE}) due to process variations.

Fig. 4 illustrates the process variation in V_{NE} and further demonstrates that using a fixed V_{ME} will result in a variation in the differences between V_{NE} and V_{ME}. This reduces the effectiveness of the margin erase test in guaranteeing the endurance specification.

Other approaches related to improving memory device circuits exist. U.S. Patents 4,809,231 and 4,903,265 to Shannon et al. describe methods for post-package testing of

one-time-programmable (OTP) EPROM memories where cells are marginally programmed to demonstrate that they are addressable. This is accomplished by applying special programming voltages such that the cell threshold changes slightly, but not enough to exceed the maximum erased specification. U.S. Patent 5,142,495 to Canepa teaches a margining circuit in an EPROM where a plurality of parallel transistors form a variable load. This effectively adjusts the current applied to the memory cell. U.S. Patent 5,369,616 to Wells et al. teaches a method where non-volatile memory is used to set memory system parameters such as threshold, word length, and addressing scheme. U.S. Patent 5,544,116 to Chao et al. teaches a method of verifying program states of Flash EPROM cells where different voltages are applied to the reference and memory cells. This controls the ratio of the currents in those cells making cell verification more accurate. U.S. Patent 5,675,537 to Bill et al. teaches a method where overerasure of memory cells in a Flash EPROM is prevented by halting erasure once a prescribed cell threshold is reached. U.S. Patent 5,870,407 to Hsia et al. teaches a method of predicting high temperature failures of Flash EPROM memory devices that reduces testing time and packaging cost. U.S. Patent 6,122,198 to Haddad et al. teaches a method for guaranteeing that an erased cell threshold voltage in a two bit per cell Flash EPROM falls within prescribed limits. This is accomplished by testing for both over and under erase conditions until all cells pass satisfactorily.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide a method that uses an internal marginal erase voltage in a Flash EPROM memory.

Another object of the present invention is to provide a method that uses an internal marginal erase voltage that is lower than the normal erase voltage in a Flash EPROM memory.

Another object of the present invention is to provide a method that uses an internal marginal erase voltage that is lower than the normal erase voltage by a fixed amount.

Another object of the present invention is to provide a method that uses an internal marginal erase voltage that is lower than the normal erase voltage by a fixed amount which tracks over processing variations and improves the endurance specification in a Flash EPROM memory.

Another object of the present invention is to provide a method that eliminates the need for a high voltage probe pad by using an internally generated marginal erase voltage in a Flash EPROM memory.

These objects are achieved by using a method where voltage-dropping components are bypassed during testing thereby effectively lowering the applied erase voltage to the marginal level desired (V_{ME}). These voltage-dropping components may be a plurality of diode-connected NMOS transistors. If a plurality of diode-connected NMOS transistors are used, the voltage applied to the flash macro is reduced by $n*V_t$, where n is the number of bypassed diode connected NMOS transistors and V_t is the threshold voltage of the NMOS transistors. In normal operation, the voltage dropping components are placed in series with the charge pump, thereby returning the voltage applied to the flash macro to the normal level (V_{NE}).

Also in accordance with the objects of the invention, a flash EPROM memory device having an internally generated margin erase voltage is achieved. The margin erase circuitry of the flash EPROM memory device comprises a charge pump with the cathode of a protective diode connected to it. The anode of the protective diode is connected to a plurality of series connected voltage dropping devices selected from a group consisting of diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes. A bias current source is connected to the opposite end of the plurality of series connected voltage dropping devices. During margin erasing, the voltage applied at the charge pump is reduced over normal erasing by bypassing one or more of the voltage dropping devices.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 schematically illustrating in cross-sectional representation a typical Flash EPROM memory cell,

Fig. 2 illustrating the variation of minimum erase voltage with the number of erasure cycles in a typical Flash EPROM memory,

Fig. 3 illustrating a schematic diagram representation of the method of marginal and normal erasure used in a typical Flash EPROM memory,

Fig. 4 illustrating the variation of normal erase voltage (V_{NE}) due to process variation and the variation in difference between the marginal erase voltage (V_{ME}) and V_{NE} in a typical Flash EPROM memory,

Fig. 5 schematically illustrating the application of the present invention to a Flash EPROM memory, and

Fig. 6 illustrating the variation of the normal erase voltage (V_{NE}) and marginal erase voltage (V_{ME}) due to process variation and that the difference between V_{ME} and V_{NE} is fixed using the circuit of the present invention in a Flash EPROM memory.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention uses the existing charge pump circuitry to generate the voltage for both normal and margin erasing. This eliminates the need for an external voltage pad to perform margin erasing and develops a margin erase voltage that better tracks over manufacturing variations.

Refer now to Fig. 5, schematically depicting the method of the present invention. The cathode of a protective diode 38 is connected to a charge pump circuitry 36. The anode of the protective diode 38 is connected to one (or more) diode-connected NMOS transistor(s) 40, for example. A diode-connected NMOS transistor is one where the drain and gate are connected. When conducting, the voltage drop across each diode-connected NMOS transistor will be equal to the transistor threshold voltage (V_t).

Referring still to Fig. 5, the important details of the present invention are illustrated. A plurality (n) of diode connected NMOS transistors 46 (46a and 46b are shown) are connected in series (i.e. the drain of transistor 46b is connected to the source of transistor 46a, the drain of transistor 46c is connected to the source of transistor 46b, etc.). The source of the diode-connected NMOS transistor(s) 40 is connected to the drain

of transistor 46a. The source of the n^{th} transistor 46n is connected to the bias current source 48. A bypass switch 50 is connected across the series connected NMOS transistors 46 such that when closed, it connects the source of transistor 40 directly to the bias current source 48. Alternately, diode-connected PMOS transistors or native NMOS transistor diodes may be used in place of the diode-connected NMOS transistors.

The function of the margin erase circuit of the present invention is now described. During normal operation, the bypass switch 50 is opened. The voltage, V_E, regulated by this regulator will be the normal erase voltage (V_{NE}), which is the sum of the voltage drops across transistors 46a-46n and 40 and the breakdown voltage (V_{bd}) of the protective diode 38. Since the voltage drop across each transistor 46a-46n and 40 is equal to V_t (threshold voltage of NMOS transistor), the normal erase voltage observed at the cathode of the protective diode 38 is given by:

$$V_{NE} = V_{bd} + V_t + n*V_t .$$

During testing, the bypass switch 50 is closed thereby bypassing transistors 46a-46n. This reduces the voltage observed at the cathode of the protective diode 38 by $n*V_t$. Thus, the margin erase voltage is given by:

$$V_{ME} = V_{bd} + V_t.$$

Refer now to Fig. 6 illustrating the variation in V_{NE} due to process tolerance. Since the characteristics of the plurality of transistors 46a-46n will follow the same process variations, the difference between V_{ME} and V_{NE} will be approximately fixed.

This allows for better prediction of the operation of the device over multiple cycles using the marginal erase method.

The present invention uses a method where a plurality of diode-connected NMOS transistors are added in series with the connection to the point of application of the erase voltage (V_E). During testing, some transistors are bypassed, thereby effectively reducing the applied erase voltage to the marginal level desired (V_{ME}). The voltage applied to the flash cells is reduced by $n*V_t$, where n is the number of diode-connected NMOS transistors bypassed and V_t is the threshold voltage of the NMOS transistors. In normal operation, the plurality of diode connected NMOS transistors are not bypassed, thereby returning the voltage applied to the flash macro to the normal level (V_{NE}). One advantage of this method over prior art methods is that the present invention allows the marginal erase voltage to track the normal erase voltage through process variations. This facilitates better prediction of device eraseability over the device life. A second advantage is the elimination of the test pad required to apply the marginal erase voltage in prior art margin erase test methods.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: